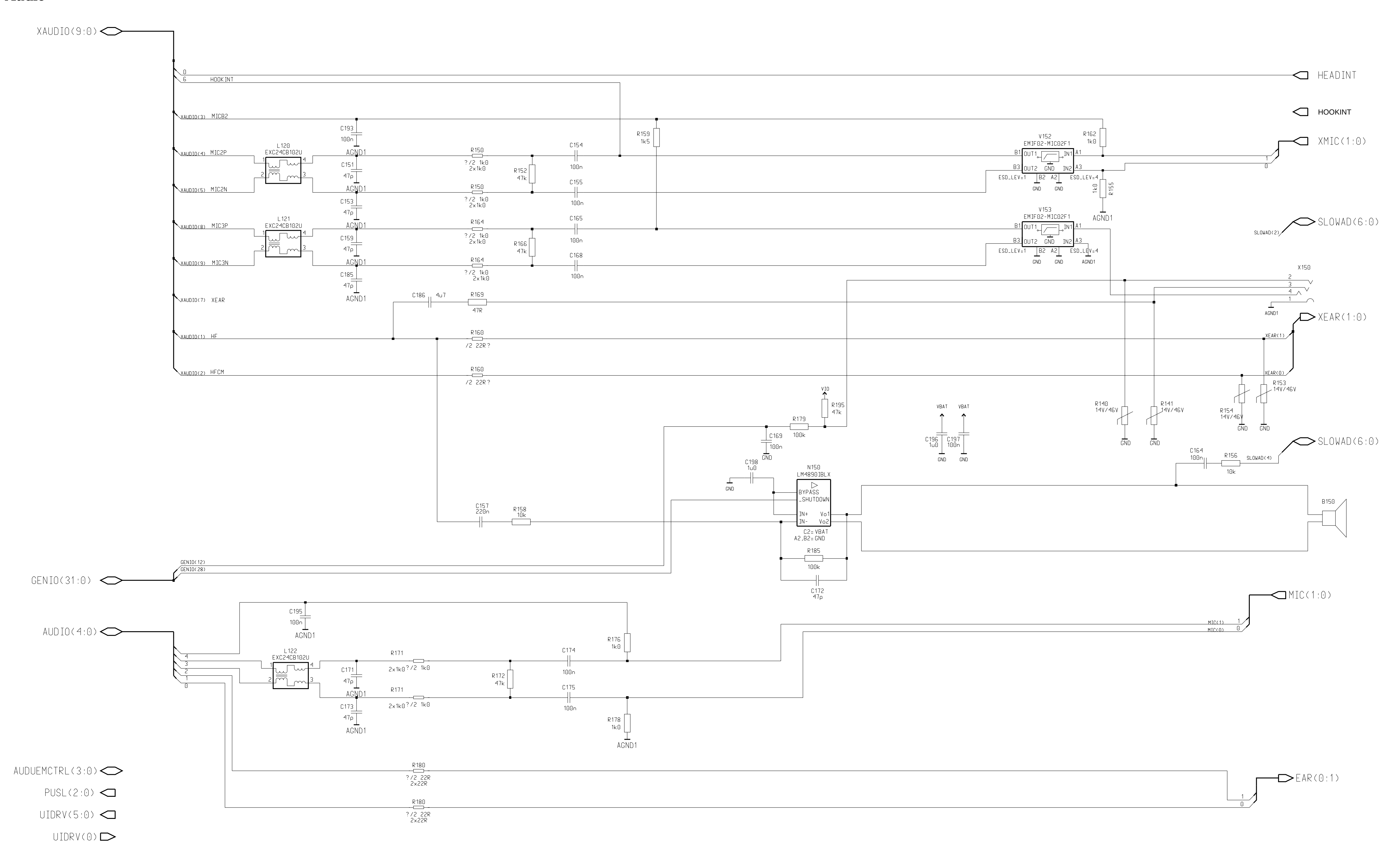
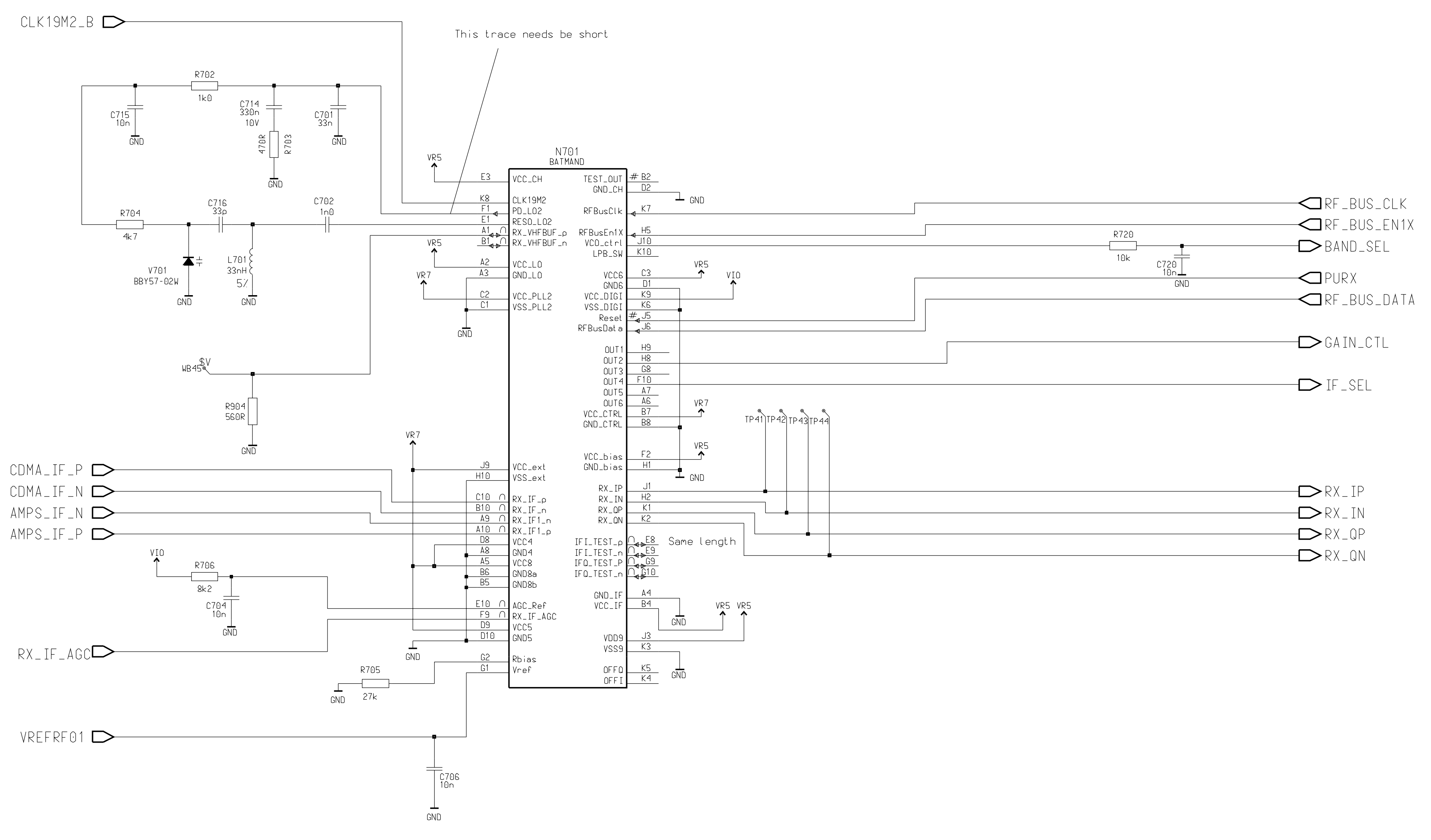
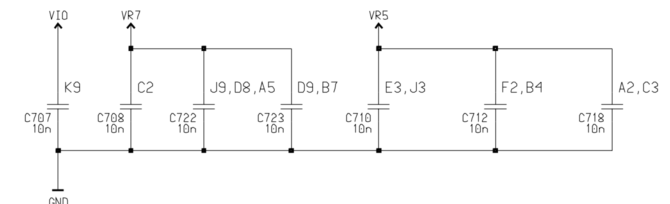
Audio



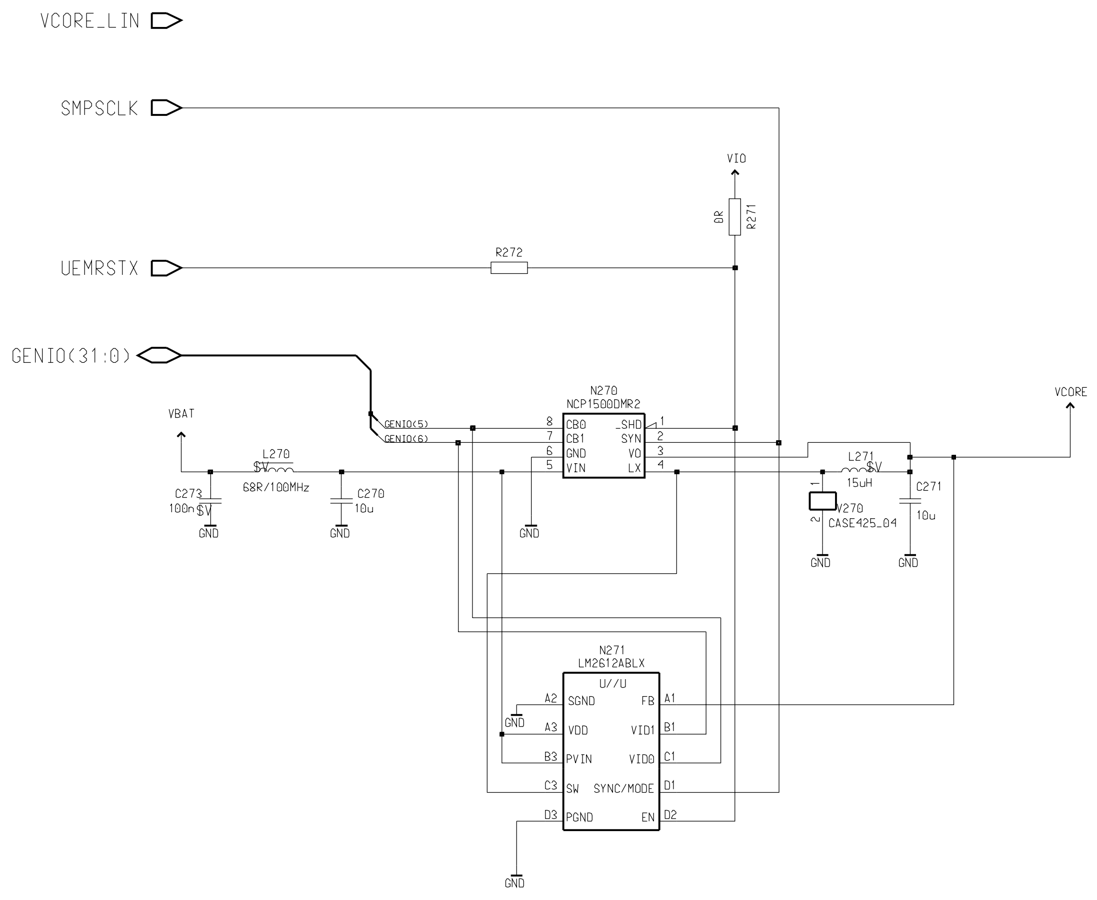
Circuit Diagram of RX (Batman)







DC-DC Converter

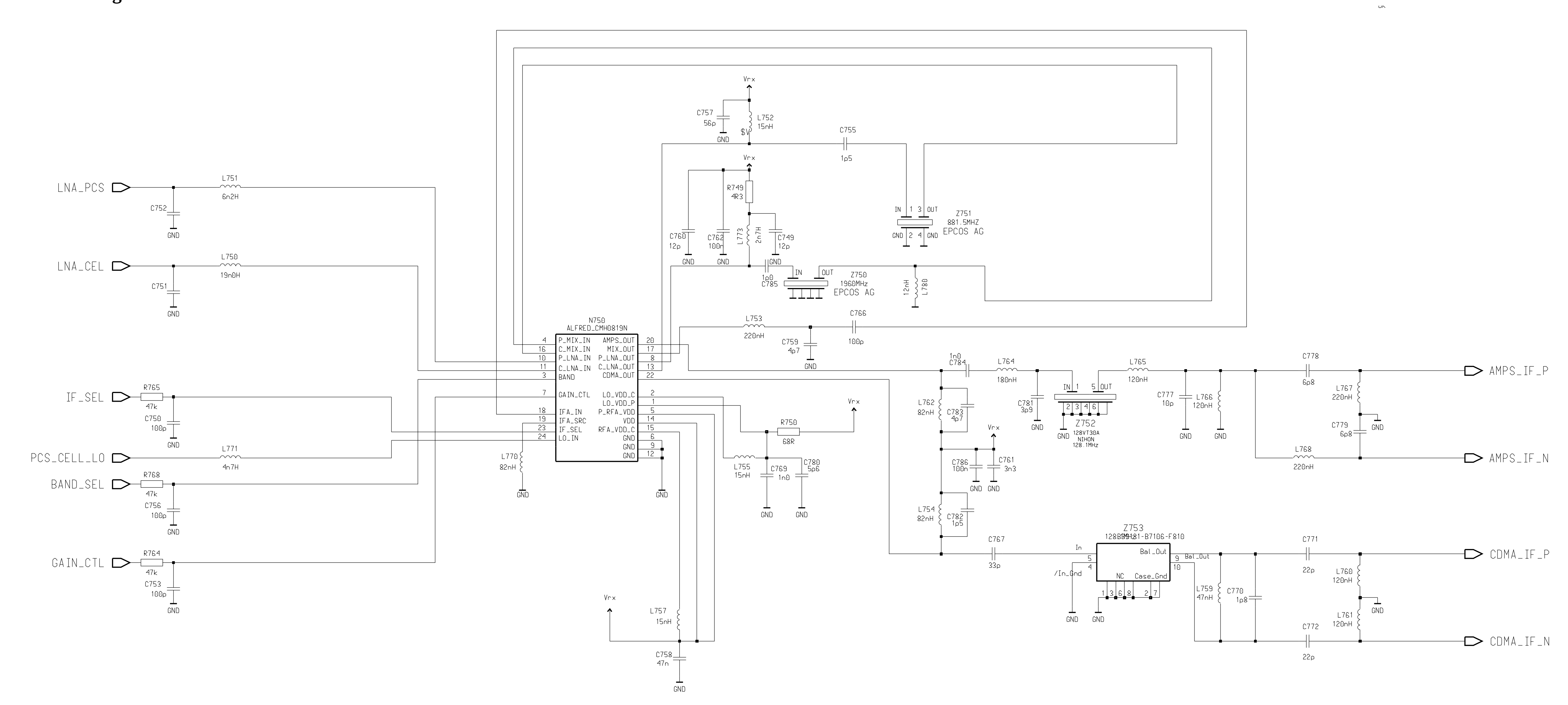


Circuit Diagram of Test and Emulator Interface



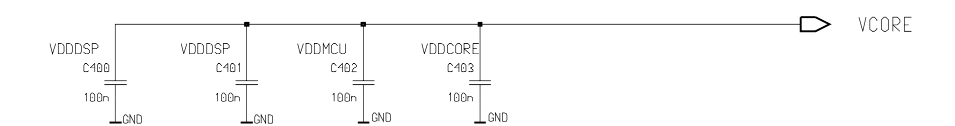


Circuit Diagram of RX front end

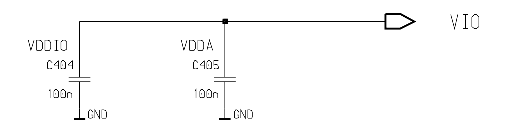


	LOGIC INPUTS		
MODES	BAND	GAIN_CTL	IF_SEL
CEL CDMA Hi Gain	0	1	0
CEL CDMA Lo Gain	0	0	0
PCS CDMA Hi Gain	1	1	0
PCS CDMA Lo Gain	1	0	0
AMPS Hi Gain	0	1	1
AMPS Lo Gain	0	0	1

UPP Decoupling Diagram



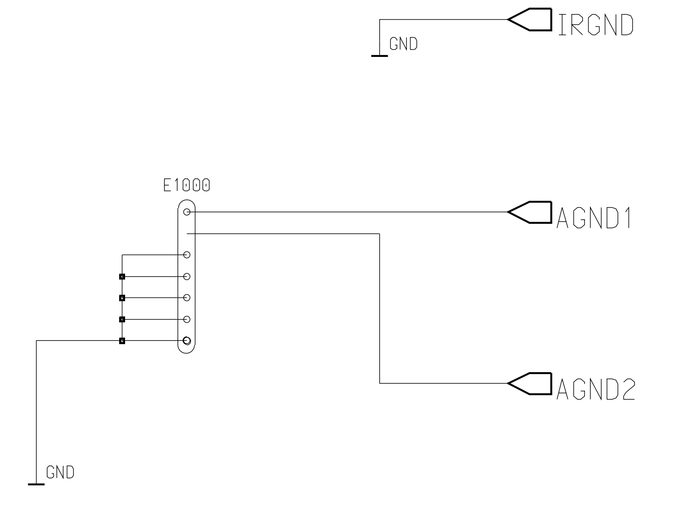
Place caps near UPP



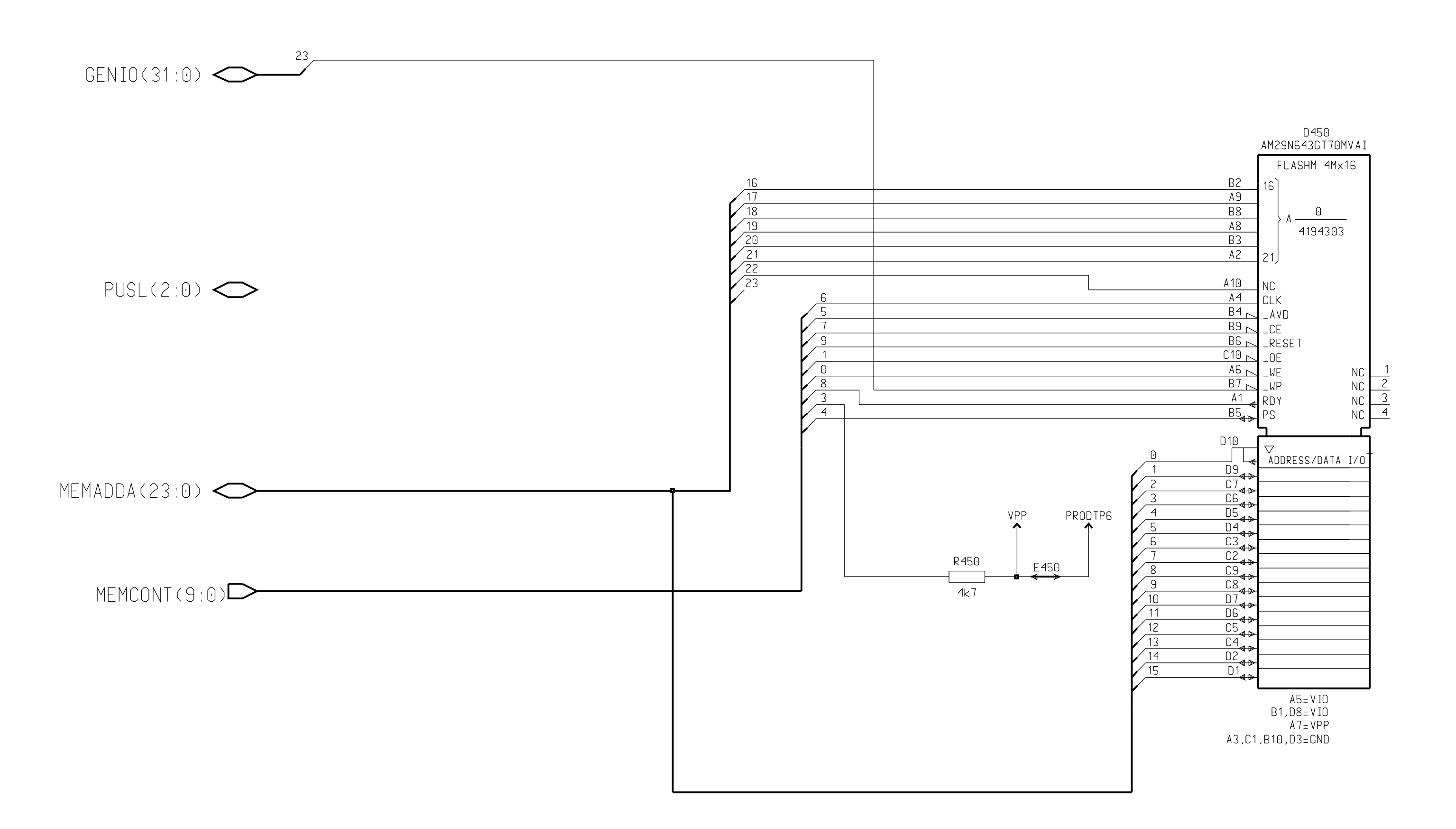
JTAG Emulator Connector and Buffers

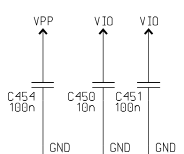


MultiGND Connecting Audio GNDs to Global GNDs

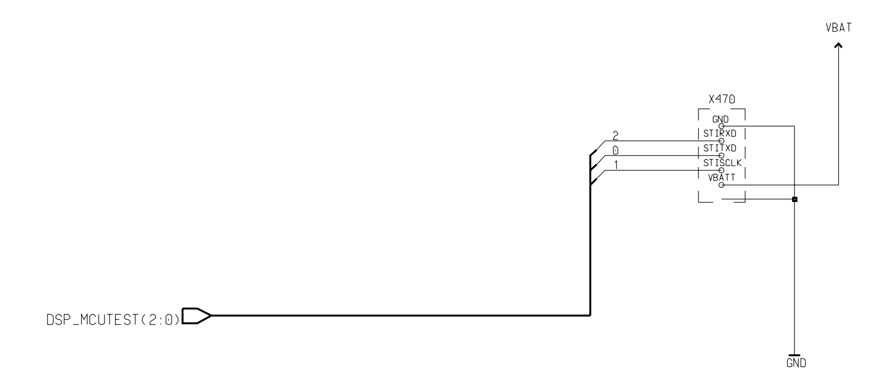


Circuit Diagram of Memory Configuration





Circuit Diagram of Ostrich Test Interface



Circuit Diagram of PA

PCS

CDMA Mode

N802
NIMBUS_9318E5.2
RFin RFout NC Vcc Vcc Iref
7,8=GND

PA_INPUT_PCS
IREF_PCS
PA_IS2000
VBAT
IREF_CEL
PA_INPUT_CEL

C808 1n0 GND
C814 100p GND
C809 15p GND
C817 10u GND
C813 47p GND
C811 68p GND
C810 1n0 GND

N801
RF9319E4.3
Vcc Iref Vcc NC RFin RFout
7,8=GND

CDMA Mode OR AMPS Mode

CELLULAR

N806
STPAC01-2A
GND1 GND1 GND1 GND2 RFin Bias DCOut Temp
B2 B3 C2 B1 C3 C1 A3 A2
VR2

R802 1k0
5n6H L802
R805 470R
R801 470R
L801 8n2H
C807 10n

Z801
SI-4BAL1.880G01-T
IN OUT

Z804
4512159
CTS
FILTER DUPLEX
TX RX ANT

LNA_PCS

R811 47R GND

CDMA Mode PCS & CELL
AMPS Mode CELL

Low Tx Power
High Tx Power

P_DET
P_REF

R803
Z805 P2 P1 DIPLEXER P3
X814
X811 Pifa FEED

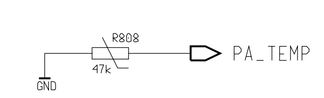
Z802
CE0538361MDCB002RD2
IN OUT

N/C
Z803 ANT
TX DUPLEX FILTER RX
D5CM-881M50-D1M4PR
824-849/869-894MHz
FUJITSU

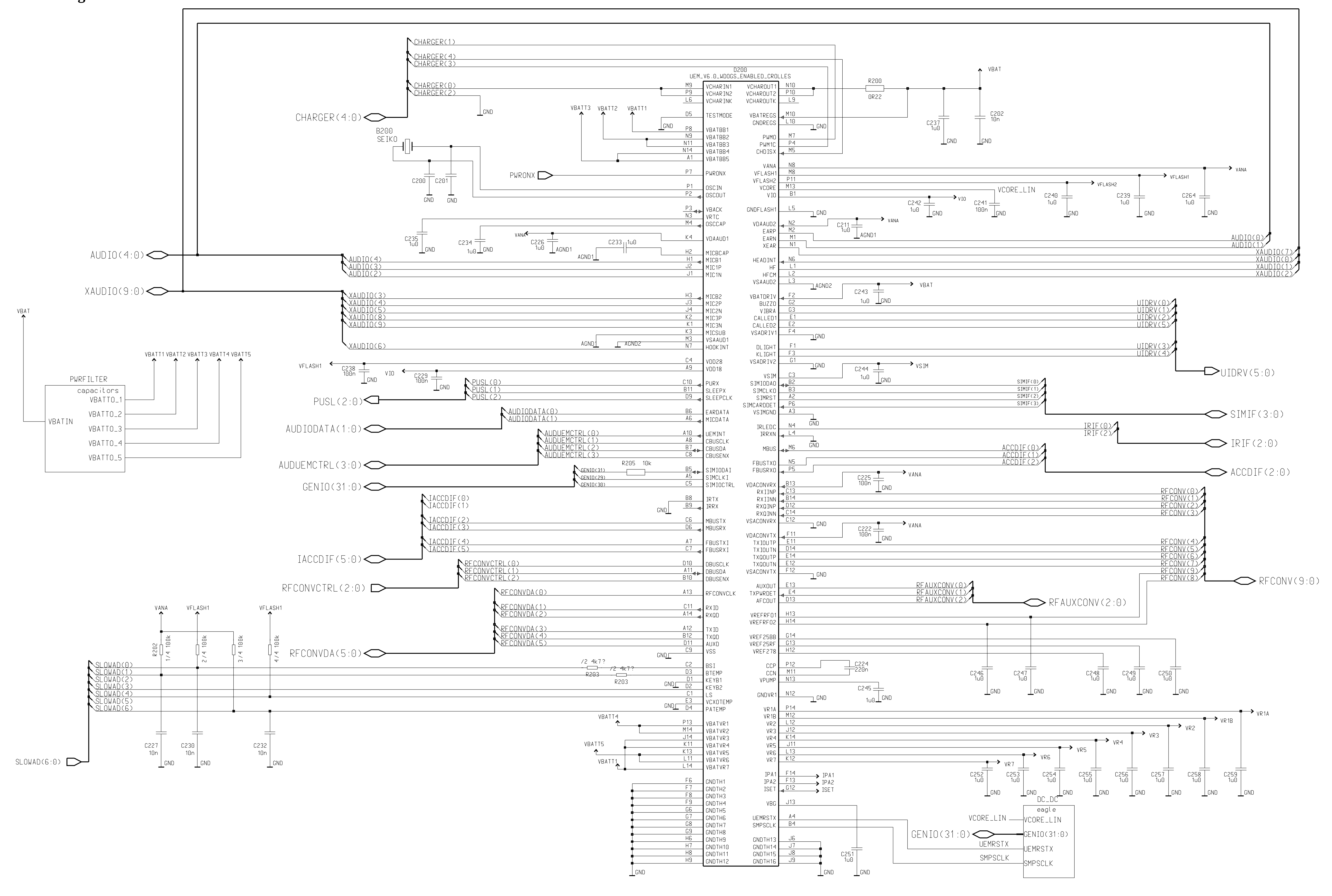
47R R810
R804

X810 Pifa GND
X812 Bottom Ant. con. stopper
C821
L805 1n0H

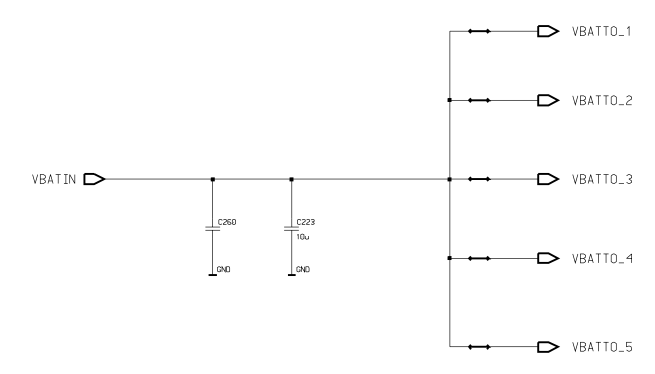
LNA_CEL



Circuit Diagram of Common Baseband

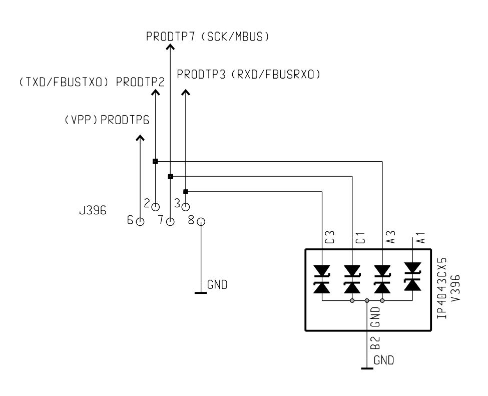


Circuit Diagram of DCT4 Power Supply

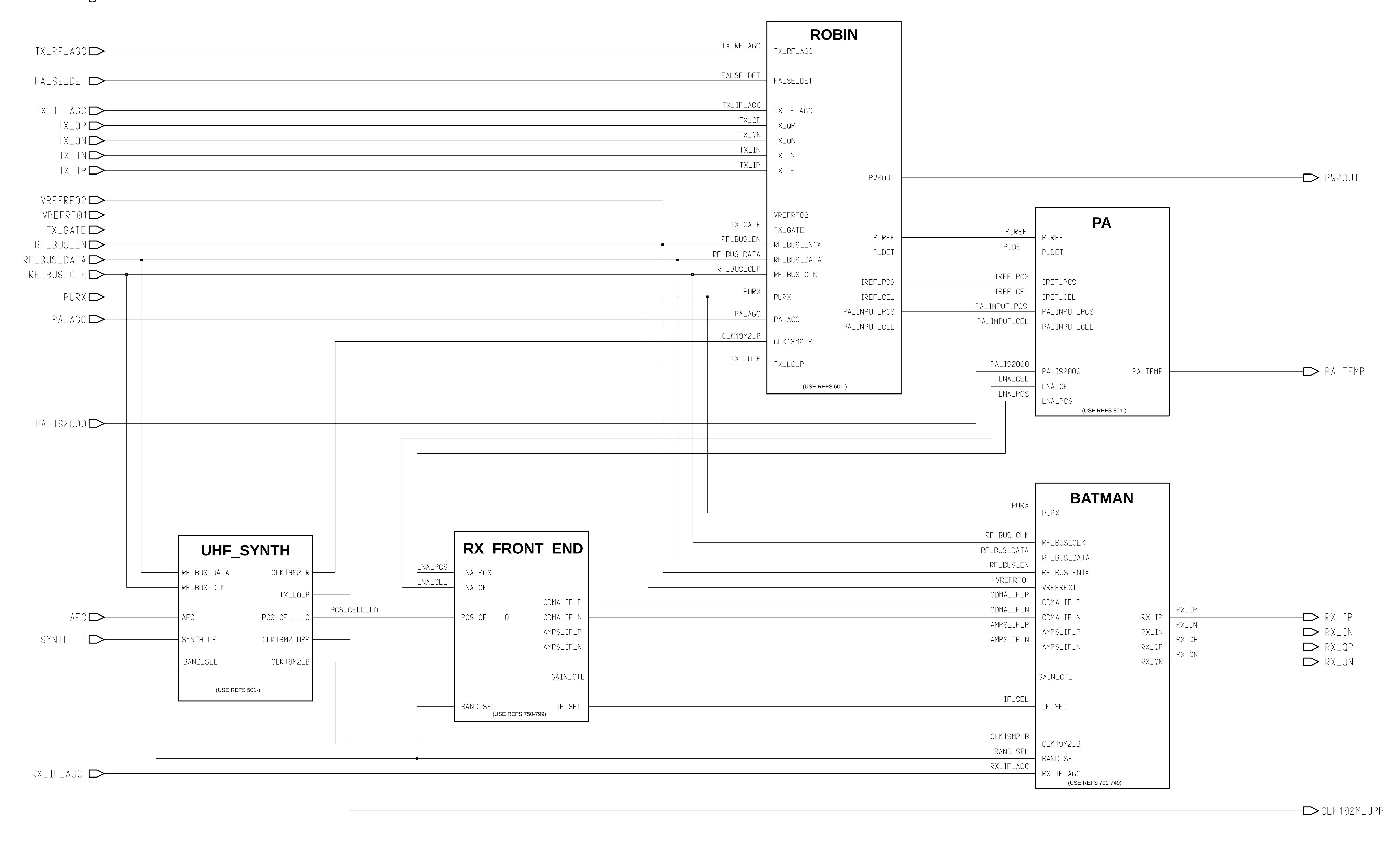


5-pin Production Test Pattern

OUT



Circuit Diagram of RF



Circuit Diagram of RF-BB Interface

GENIO(31:0)

13 --> FAST_AGC
03 --> PA_IS2000
25 --> SYNTH_LE
09 --> RX_IF_AGC
26 --> TX_RF_AGC
07 --> TX_IF_AGC
11 --> PA_GAIN
08 --> TX_GATE
21 --> WHIP_DET

R435 4k7
C428 10n GND
C435 10n GND
R433 1k0
R434 4k7
C426 10n GND
C427 1n0 GND
C429 33n
V420 DTC143ZETL IN R1 4k7 R2 47k OUT GND MODEL GND
R427 1k0
R428 4k7
C422 10n GND
C423 1n0 GND
C430 33n
V421 DTC143ZETL IN R1 4k7 R2 47k OUT GND MODEL GND
R430 1k0
R431 4k7
C424 10n GND
C425 1n0 GND
C431 33n
V422 DTC143ZETL IN R1 4k7 R2 47k OUT GND MODEL GND

09 26 07 11 03 25 08 21 12 13
GENIO_O(31:0)

RFCONV(9:0) → RFCONV_O(9:0)

8 --> VREFRF02 8
9 --> VREFRF01 9
0 <-- RX_IP 0
1 <-- RX_IN 1
2 <-- RX_QP 2
3 <-- RX_QN 3
4 --> TX_IP 4
5 --> TX_IN 5
6 --> TX_QP 6
7 --> TX_QN 7

RFAUXCONV(2:0) → RFAUXCONV_O(2:0)

0 --> AUXOUT 0
1 <-- PWROUT 1
2 --> AFC 2

RFCLK <-- 19.2_MHZ RFCLK_I
RFCLKGND <-- 19.2_MHZGND RFCLKGND_I

PUSL(2:0) → PUSL_O(2:0)

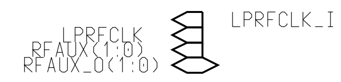
0 --> PURX 0
1 --> SLEEPX 1
2 --> SLEEPCLK 2

SLOWAD(6:0) → SLOWAD_O(6:0)

3 <-- FALSE_DET 3
6 <-- PA_TEMP 6

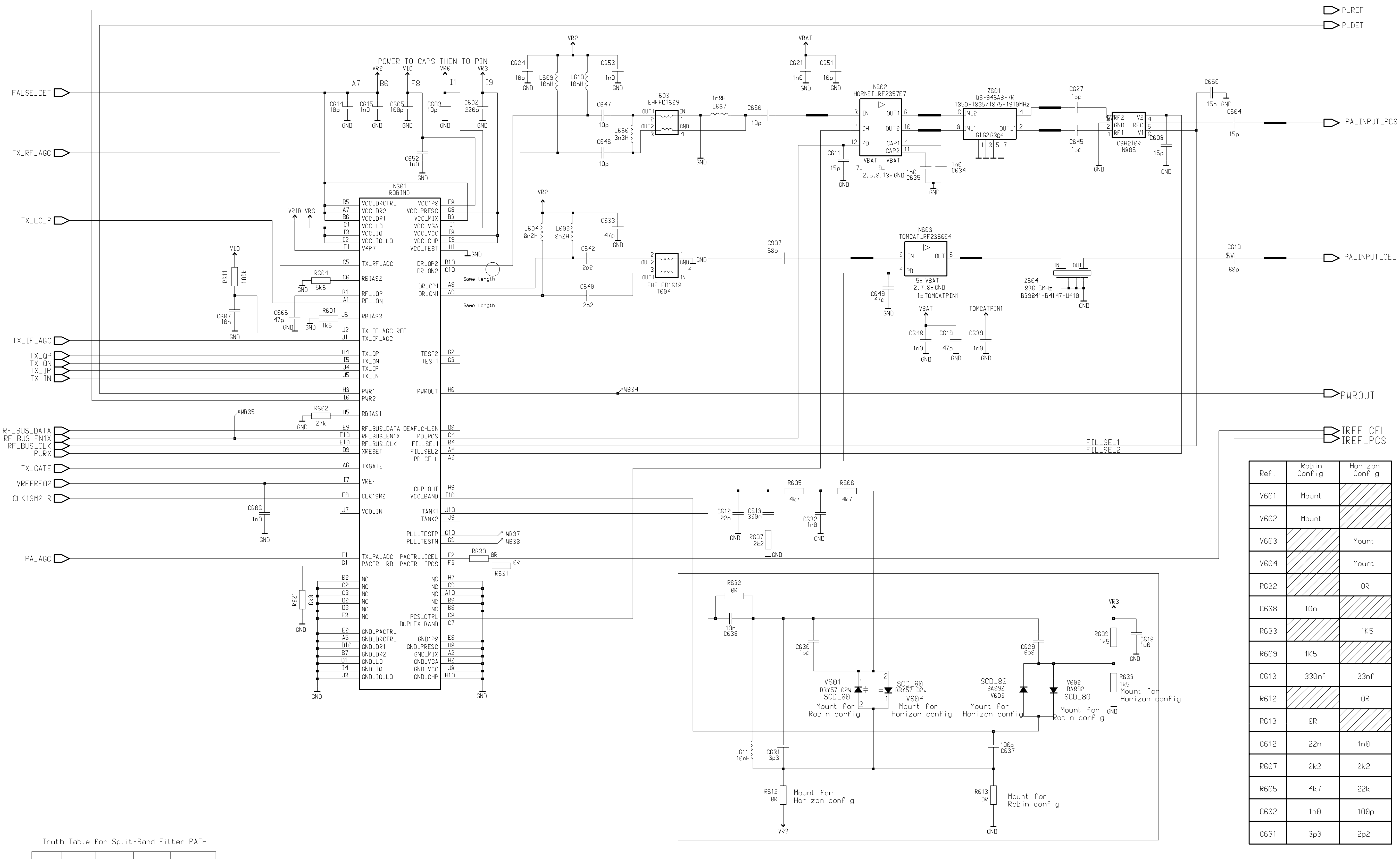
RFICCNTRL(2:0) → RFICCNTRL_O(2:0)

0 --> RFBusClk 0
1 <-> RFBusData 1
2 --> RFBusEn1X 2



LPRFCLK_I

Circuit Diagram of Robin



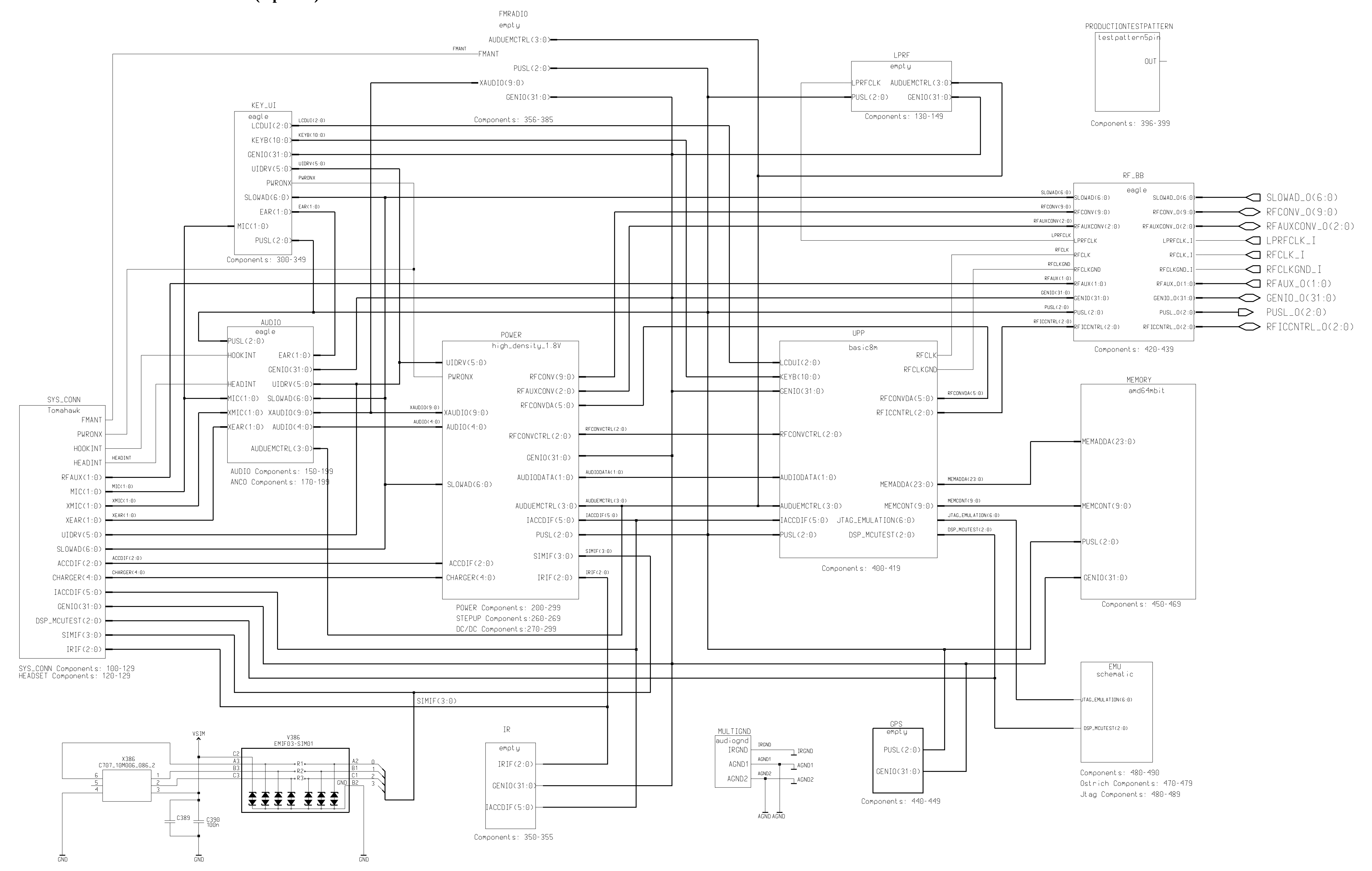
Ref.	Robin Config	Horizon Config
V601	Mount	
V602	Mount	
V603		Mount
V604		Mount
R632		0R
C638	10n	
R633		1K5
R609	1K5	
C613	330nf	33nf
R612		0R
R613	0R	
C612	22n	1n0
R607	2k2	2k2
R605	4k7	22k
C632	1n0	100p
C631	3p3	2p2

Truth Table for Split-Band Filter PATH:

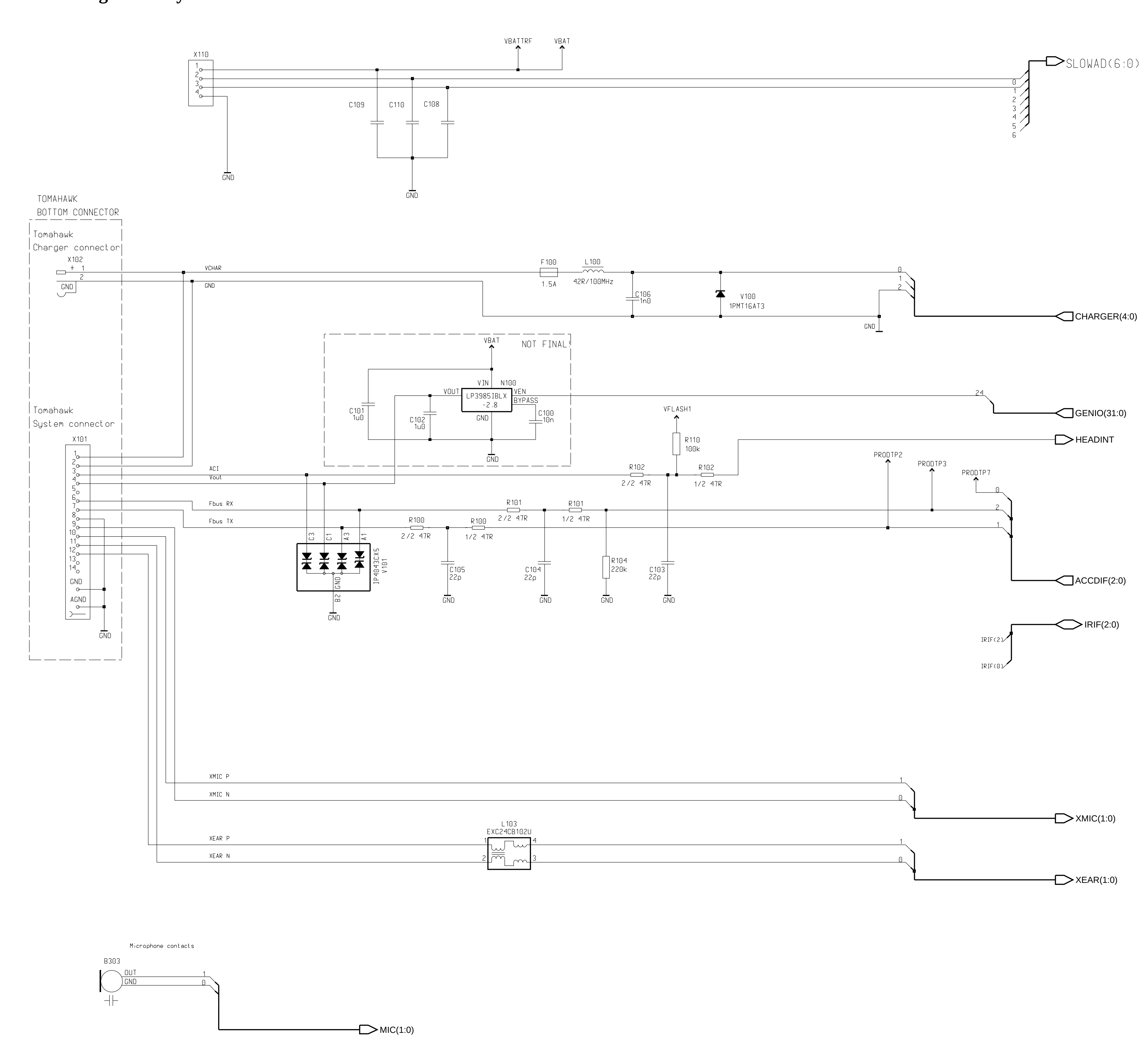
DRV CNTL	DRV OUT STATE	VCONT1	VCONT2	SWITCH IN STATE
0 volt	RFOUT1	0 volt	2.7 volt	RFI1
2.7 volt	RFOUT2	2.7 volt	0 volt	RFI2

	VCO_BAND
Cell band	low (shorted to ground)
PCS band	tri-stated (open circuit)

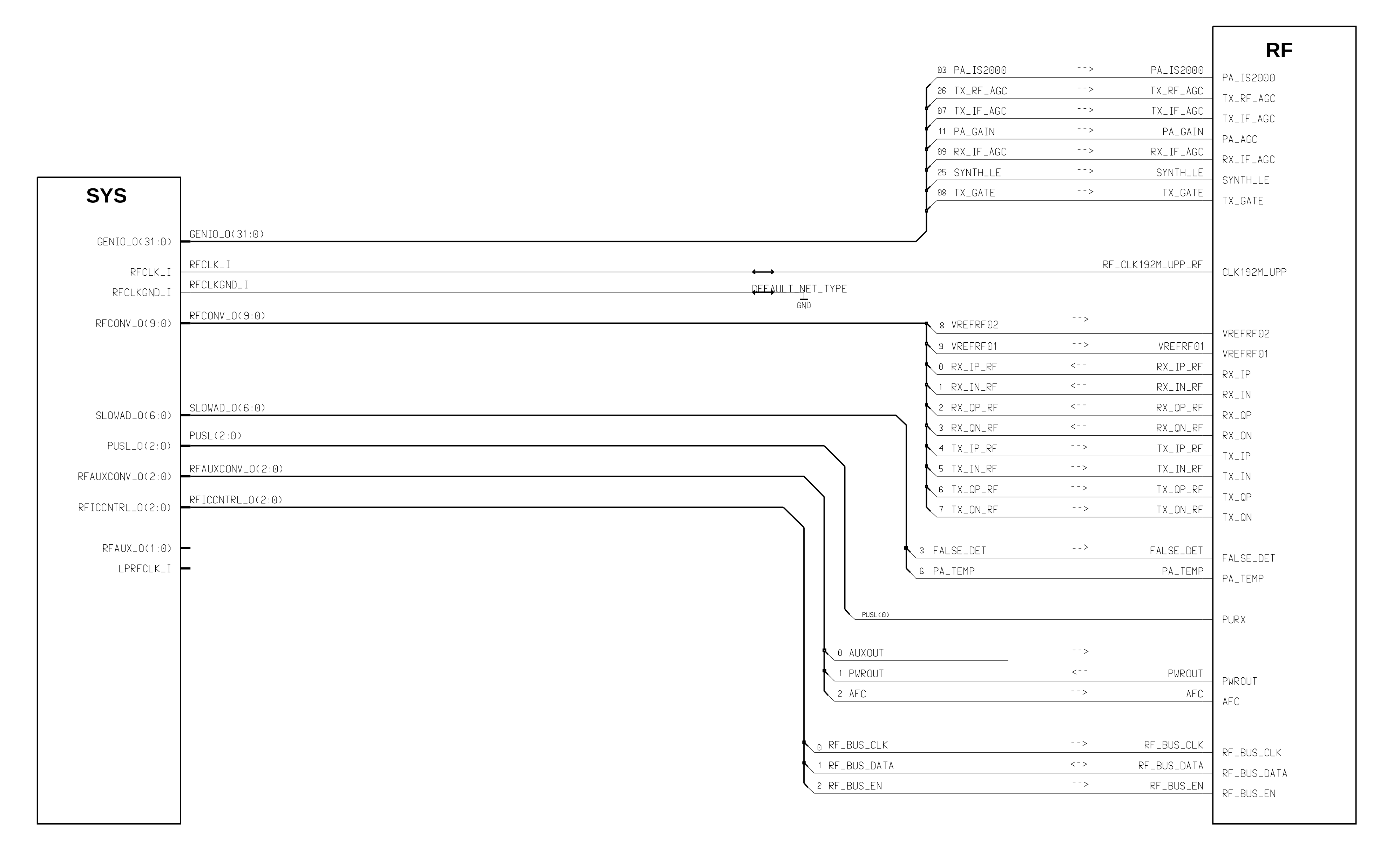
DCT4 Common Baseband Schematic (top level)



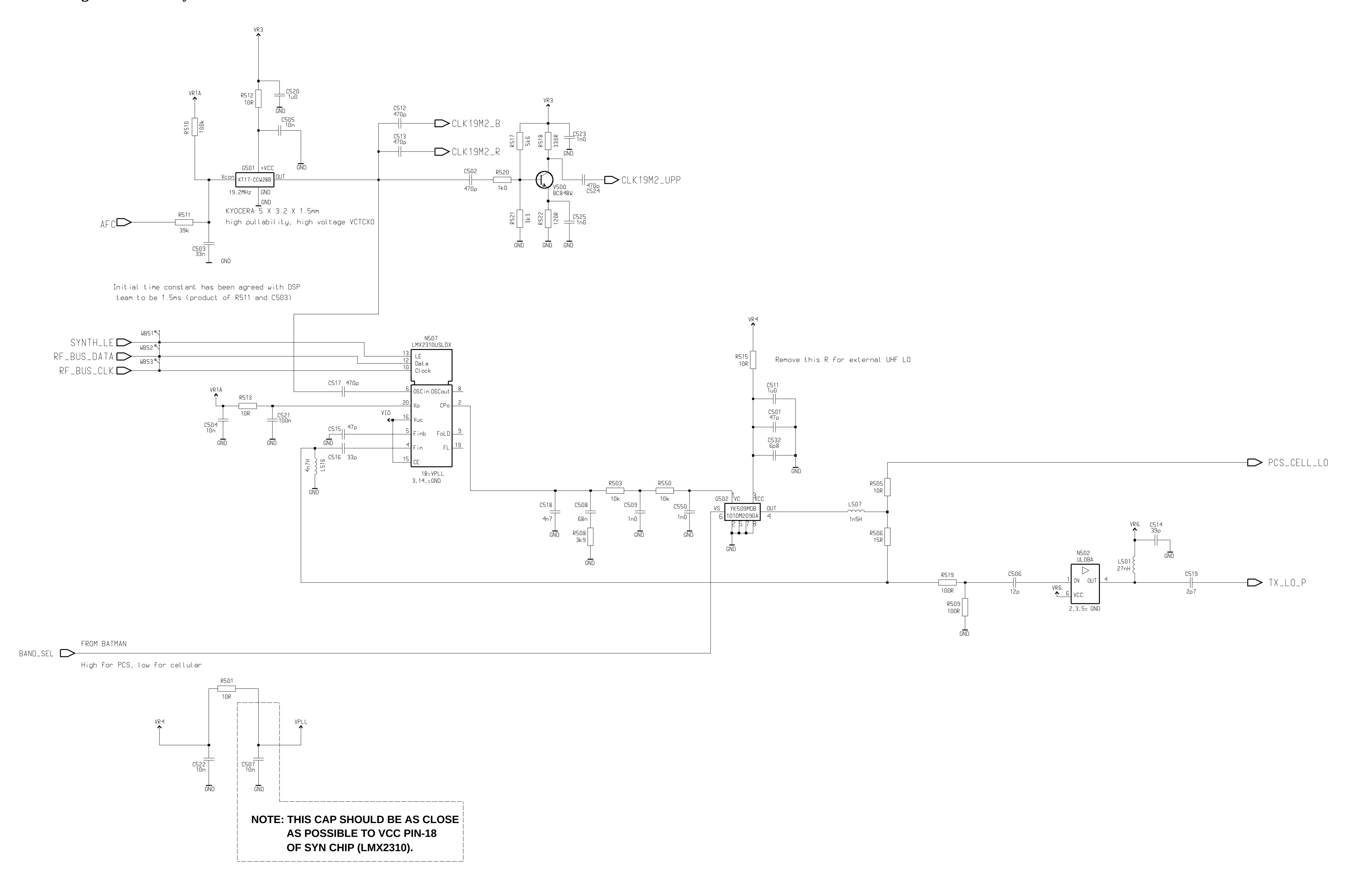
Circuit Diagram of System Connector



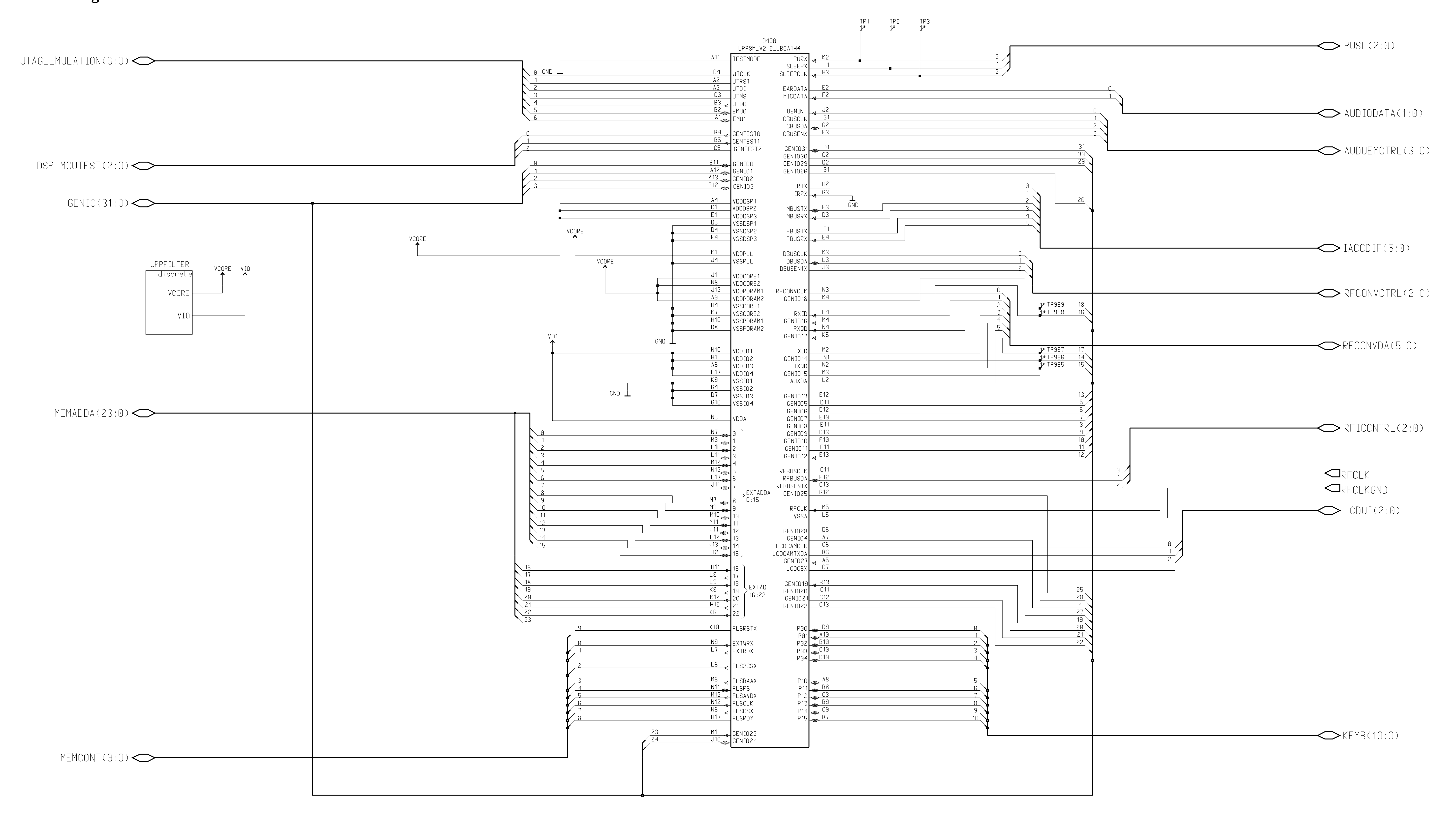
Circuit Diagram of Top Level



Circuit Diagram of UHF Synthesizer

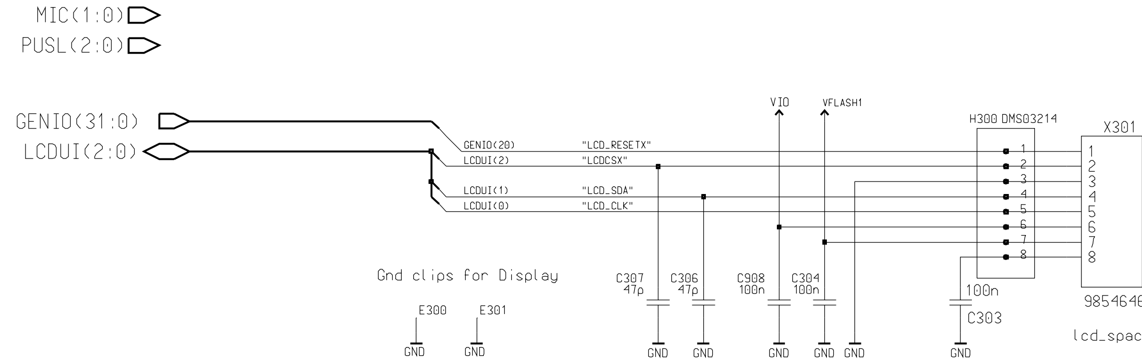


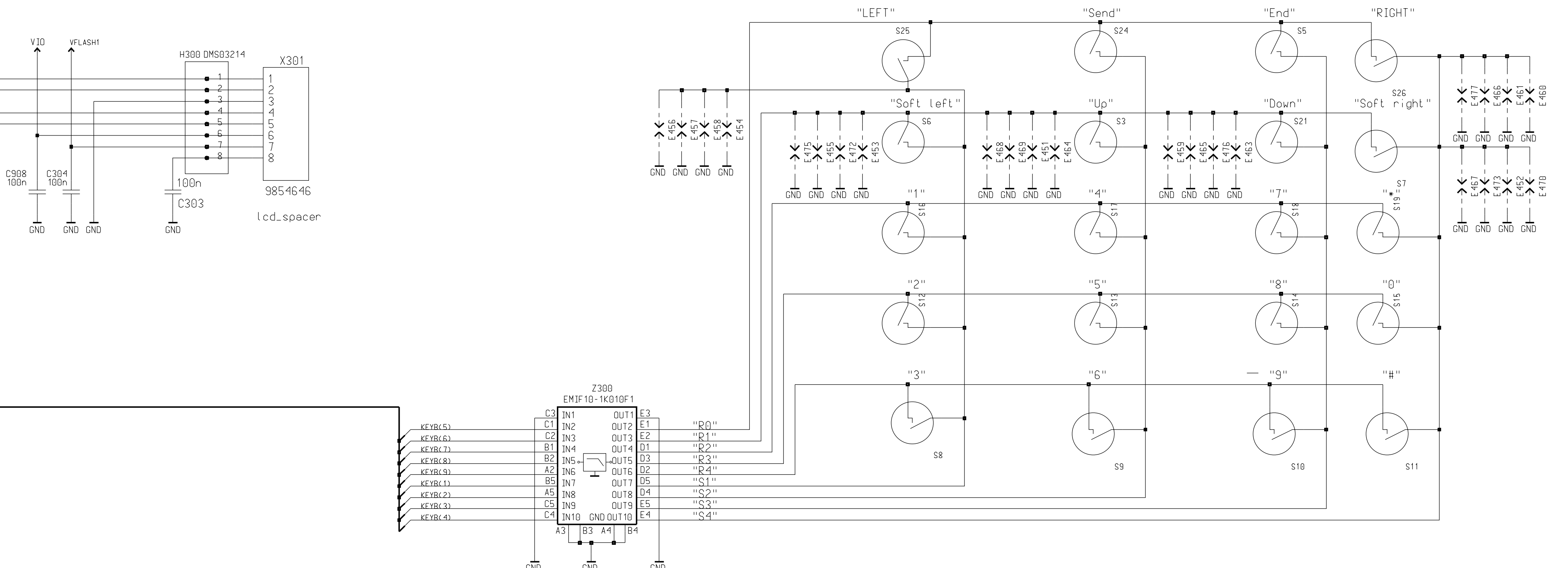
Circuit Diagram of DCT4 UPP



User Interface

SLOWAD(6:0)
MIC(1:0)
PUSL(2:0)

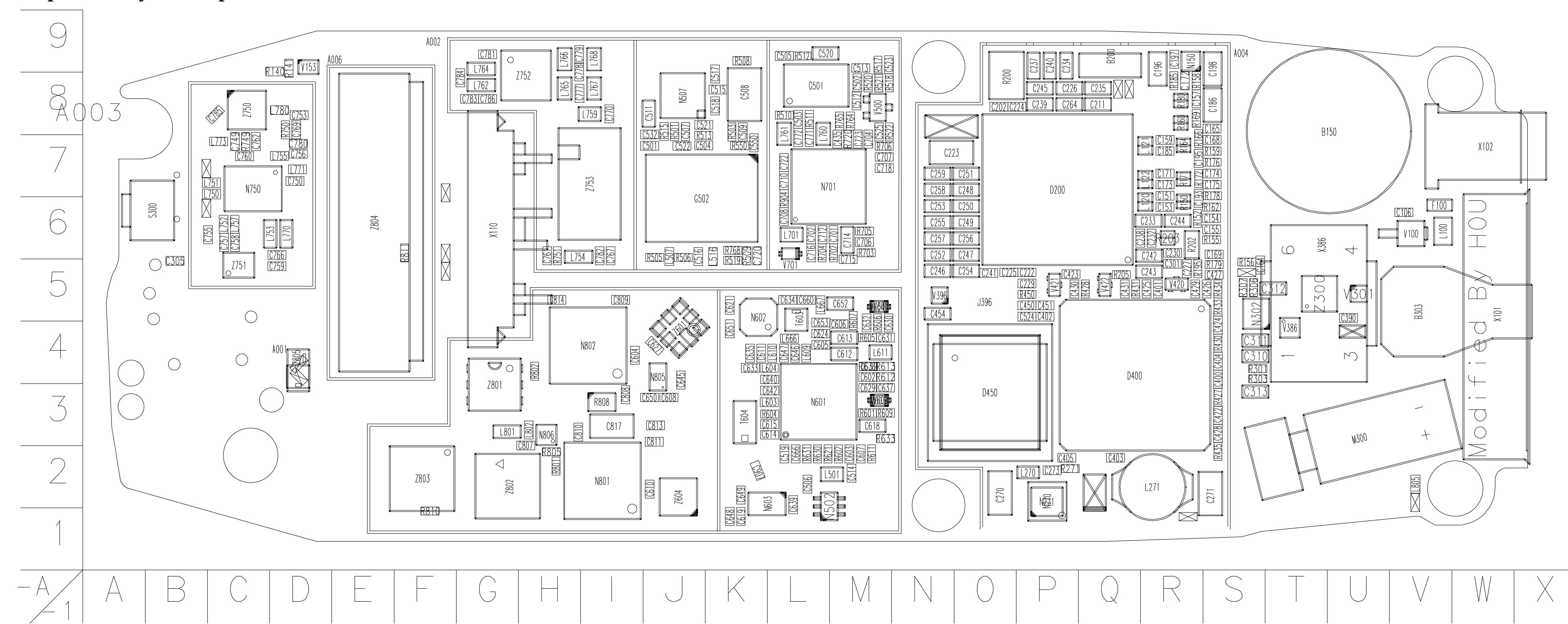




UIDRV(5:0)
"VIBRA"
"DLIGHT"
"KLIGHT"
VBAT
KHN4NB1H
M300
R306
1k0
N302
LM2795BLX
C311 1u0
C312 1u0
C310 1u0
180R R307
C313 1u0
220R R301
220R R303
CL-191WB-D-T
V312 V313 V314 V315
CL-270WB-D-T
V316 V317
DISPLAY
KEY
"PWM CONTROL MUST BE APPLIED TO DLIGHT AND KLIGHT WHEN VBATT > 3.4!"

"PWRON KEY SWITCH"
READ COMPONENT INFO!
PWR
S300
PWRONX
C305 100n
"NOT SMD COMPONENT"
R302
V301
IP4043CX5
VFLASH2
X300
SLOWAD(4)
C301 10n
"DCT3 SPEAKER"
"NOT SMD COMPONENT"
EAR(1:0)
GND

Component Layout - Top



Component Layout - Bottom

